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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,217	12/18/2001	Igor Liokumovich	10559-544001 / P12564	5026

20985 7590 02/07/2006

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EXAMINER	
GUILL, RUSSELL L	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/025,217	LIOKUMOVICH ET AL.	
	Examiner	Art Unit	
	Russell L. Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5 and 7-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5 and 7-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to an Amendment filed December 13, 2005. Claims 1, 7-9, 11, 14 and 16-22 were amended. Claims 2 and 6 were canceled. Claims 1, 3-5 and 7 - 22 have been examined. Claims 1, 3-5 and 7 - 22 have been rejected.

Response to Remarks

2. Regarding **claims 2, 7, 8, 11, 14, 15, 16, 18, 21 and 22** rejected under 35 USC § 112:

   2.1. The claims were amended to correct the issues, and the rejections are withdrawn.

3. Regarding independent **claims 1, 9 and 16** rejected under 35 USC § 103(a):

   3.1. The claims were amended to require "an operating system executing on the host machine also supports a full platform simulator that includes device models." The Applicant argues that Bugnion shows device emulators and I/O emulation modules for use with a virtual machine monitor (VMM), but in contrast the claimed invention requires the operating system on the host machine (not the VMM) to provide the full platform simulator. The Examiner finds this argument persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made as described in the rejections below.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4.1. **Claims 3, 7 and 8** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention:

4.1.1. **Claim 3** recites "the same addresses." The phrase has insufficient antecedent basis. For the purpose of claim examination, the phrase is interpreted as "a same addresses."

4.1.2. **Claims 7 and 8** recite, "the system of claim 6." Claim 6 was canceled. For the purpose of claim examination, the phrase is interpreted as "the system of claim 1."

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for

the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. **Claims 1, 3, 4, 9, 10, 11, 13, 16, 17, 18 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Devine (U.S. Patent 6,397,242, May 28, 2002) in view of Klaiber (Klaiber, Alexander; "The Technology Behind Crusoe Processors", January 2000, www.transmeta.com/pdfs/paper_aklaiber_19jan00.pdf), further in view of Bugnion (U.S. Patent 6,496,847).

7.1. Regarding claims 1, 9, and 16:

7.1.1. Devine appears to teach a monitor that translates the machine instructions into translated code (*column 8, lines 1 - 4; column 21, lines 60 - 67; and column 22, lines 1 - 21*).

7.1.2. Devine appears to teach a virtual machine that executes the translated code stored in memory (*column 10, lines 51 - 54; and column 22, lines 7 - 8; and column 25, lines 23 - 46 [especially lines 36 - 46]*).

7.1.3. Devine appears to teach a kernel that detects exceptions occurring in the virtual machine and transfers control between the virtual machine and the monitor according to the type of exception (*column 14, lines 56 - 62; and column 17, lines 33 - 39; and column 17, lines 44 - 50; and column 22, lines 45 - 55*).

7.1.4. Devine does not specifically teach a monitor that translates the machine instructions into translated code, *the monitor modifying original values in a descriptor table to prevent the translated code from being accessed, thereby preventing the translated code from being modified*.

7.1.5. Devine does not specifically teach a monitor wherein an operating system executing on the host machine also supports a full platform simulator that includes simulation modules and device models.

7.1.6. Klaiber appears to teach the monitor modifying original values in a descriptor table to prevent the translated code from being accessed, thereby preventing the translated code from being modified (*Klaiber, page 14, section "Coping with Self-modifying code", fourth sentence*).

7.1.7. Bugnion appears to teach an operating system executing on the host machine also supports a full platform simulator that includes simulation modules and device models (*figure 2, all elements; and column 6, lines 55 - 67, and column 7, lines 1 - 10; and column 2, lines 37 - 65*).

7.1.8. The motivation to use the art of Bugnion with the art of Devine is that Bugnion and Devine are co-inventors on the cited patents, and the Devine patent incorporates the Bugnion application by reference (*Devine, column 24, lines 15 - 17*), and finally, using a device emulator allows portability of the virtual machine monitor across a wide range of platforms (*Bugnion, column 4, lines 30 - 35; and column 7, lines 21 - 30*).

7.1.9. The motivation to use the art of Klaiber with the art of Devine is the benefit recited in Klaiber of a solution that combines strong performance with remarkably low power consumption (*Klaiber, page 3, section "Summary", first sentence*). Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Klaiber and the art of Bugnion with the art of Devine to produce the claimed inventions.

7.2. **Regarding claims 3, 11 and 18**:

7.2.1. Devine appears to teach that the translated code and the original machine instructions access the memory using a same set of addresses as a set of addresses used by the original machine instructions (*column 10, lines 50 - 55; and column 1, lines 45 - 67*).

7.2.1.1. Regarding (*column 10, lines 50 - 55; and column 1, lines 45 - 67*); since the virtual machine directly executes instructions on the underlying hardware, it is obvious that the translated code and the original machine instructions access the memory using a same set of addresses as a set of addresses used by the original machine instructions.

7.3. Regarding claim 4:

7.3.1. Devine appears to teach that the monitor further includes an auxiliary simulator that executes the machine instructions (*column 21, lines 61 - 67; and column 22, lines 1 - 6*).

7.3.1.1. Regarding (*column 21, lines 61 - 67; and column 22, lines 1 - 6*); since the translator calls the VMM to execute certain machine instructions, it is obvious that the monitor further includes an auxiliary simulator that executes the machine instructions.

7.4. Regarding claims 13 and 20:

7.4.1. Devine does not specifically teach that the monitor modifies a descriptor table to prevent the translated code from being modified.

7.4.2. Klaiber appears to teach that the monitor modifies a descriptor table to prevent the translated code from being modified (*Klaiber, page 14, section "Coping with Self-modifying code", fourth sentence*).

7.5. Regarding claims 10 and 17:

7.5.1. Devine does not specifically teach that the host operating system also supports a full platform simulator that includes device models, and simulates a device.

7.5.2. Bugnion appears to teach that the host operating system also supports a full platform simulator that includes device models, and simulates a device (*figure 5, element 520; and figure 3,*

element 300; and column 20, lines 11 - 20; and column 16, lines 10 - 61; and column 7, lines 20 - 26).

8. **Claims 5, 12 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Devine and Klaiber and Bugnion as applied to **claims 1, 3, 4, 9, 10, 11, 13, 16, 17, 18 and 20** above, further in view of Lawton (Lawton, Kevin; "Running multiple operating systems concurrently on an IA32 PC using virtualization techniques", www.anticracking.sk/EliCZ/import/Vx86.txt).

8.1. Devine as modified by Klaiber and Bugnion teach a system, method and computer program product for simulating machine instructions on a host machine as described in **claims 1, 3, 4, 9, 10, 11, 13, 16, 17, 18 and 20** above.

8.2. **Regarding claims 5, 12 and 19**:

8.3. Devine does not specifically teach that the monitor replaces one of the machine instructions with a capsule if the machine instruction accesses a system state of a central processing unit of the host machine.

8.4. Lawton appears to teach that the monitor replaces one of the machine instructions with a capsule if the machine instruction accesses a system state of a central processing unit of the host machine (*page 3, section "CHALLENGE ON THE IA32", paragraphs 1 - 3*).

8.4.1. Regarding (*page 3, section "CHALLENGE ON THE IA32", paragraphs 1 - 3*); trapping out is equivalent to a capsule.

8.5. The motivation to use the art of Lawton with the art of Devine and Klaiber and Bugnion would have been the benefit recited in Lawton to run a primary PC operating system and related software while retaining the ability to concurrently run software engineered for a different PC

operating system (*page 1, section "THE RATIONALE FOR VIRTUALIZATION", first paragraph*). Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Lawton with the art of Klaiber, Bugnion and Devine to produce the claimed inventions.

9. **Claims 7, 8, 14, 15, 21 and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Devine and Klaiber and Bugnion as applied to **claims 1, 3, 4, 9, 10, 11, 13, 16, 17, 18 and 20** above, further in view of Stallings (Stallings, William; "Operating systems: internals and design principles", 1998, Prentice-Hall).

9.1. Devine as modified by Klaiber and Bugnion teach a system, method and computer program product for simulating machine instructions on a host machine as described in **claims 1, 3, 4, 9, 10, 11, 13, 16, 17, 18 and 20** above.

9.2. **Regarding claims 7, 14, and 21**:

9.2.1. Devine does not specifically teach that the monitor modifies the descriptor table to remove a portion of a segment that overlaps with the memory storing the translated code.

9.2.2. Stallings appears to teach that the monitor modifies the descriptor table to remove a portion of a segment that overlaps with the memory storing the translated code (*page 334, section labeled "Segmentation", sub-section labeled "Virtual Memory Implications", second paragraph, especially item number 1, sentence 3; and pages 307 - 309 section 7.4 Segmentation*).

9.2.2.1. Regarding (*page 334, section labeled "Segmentation", sub-section labeled "Virtual Memory Implications", second paragraph, especially item number 1, sentence 3; and pages 307 - 309 section 7.4 Segmentation*); since the advantage of segmentation was that the operating system will shrink a segment as needed, it would have been obvious that the

monitor modifies the descriptor table to remove a portion of the segment that overlaps with the memory storing the translated code.

9.2.3. The motivation to use the art of Stallings with the art of Devine is the advantage recited in Stallings that segmentation simplifies the handling of growing data structures, and the operating system will expand or shrink the segment as needed (*page 334, section labeled "Segmentation", sub-section labeled "Virtual Memory Implications", second paragraph, especially item number 1, sentence 3*). Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Stallings with the art of Klaiber, Bugnion and Devine to produce the claimed inventions.

9.3. Regarding claim 8, 15 and 22:

9.3.1. Devine does not specifically teach that the monitor modifies the descriptor table to replace a segment with a substitute segment, which, when accessed, causes an exception to be generated.

9.3.2. Stallings appears to teach that the monitor modifies the descriptor table to replace a segment with a substitute segment, which, when accessed, causes an exception to be generated (*page 335, section labeled "Organization", first paragraph, especially the sentence that starts with "Because only some of the segments of a process may be in main memory . . . "; and page 324, figure 8.2b; and pages 324 - 325, section labeled "Paging"; and pages 319 – 320, section 8.1 "Hardware and Control Structures", especially page 320, the paragraph that starts with "Let us consider . . ."*).

9.3.3. The motivation to use the art of Stallings with the art of Devine is the benefit recited in Stallings that it is not necessary for all of the segments to be in memory during execution (*page 319, section 8.1 "Hardware and Control Structures"*).

10. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the Applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russ Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday - Friday 9:00 AM - 5:30 PM.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG

Paul L. Rodriguez 2/3/06
Primary Examiner
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